ABSTRACT

This paper presents interleaved buck converters using a switching rule based on winner-take-all nonlinearity. The switching rule can realize flexible phase control and the system can generate various interesting synchronous phenomena. Using a simple piecewise constant model, we clarify parameters conditions for existence and stability of the phenomena. We also discuss current sharing and ripple reduction for practical applications.

1. INTRODUCTION

Parallel connection of switching converters [1]-[6] is an interesting technique from both practical and fundamental viewpoints. First, the converters share the input current. The sharing can provide lower voltages with higher current capabilities for microprocessors; and can improve reliability, fault tolerance, and so on [2, 5, 7]. Second, ripple reduction of the output current is possible. It is convenient to reduce size and losses of the filtering stages; and also can decrease switching and conduction losses and EMI levels [1, 3, 4]. In order to reduce the ripple some efficient phase control techniques are proposed [3, 4, 5]. Third, the switching converters are important switched dynamical systems which can exhibit interesting nonlinear phenomena [6, 8, 9, 10, 11]. The nonlinear switching rule can cause interesting bifurcation phenomena, and the phenomena can be studied in terms of power electronics. In the previous literatures single converters have been studied well, however, many open problems remain for interleaved converters, e.g., analysis of synchronous phenomena and related bifurcation.

In this paper we present interleaved buck converters using a switching rule based on winner-take-all (WTA) nonlinearity. The switching can realize flexible phase control and the system can generate various interesting synchronous phenomena. In order to analyze the dynamics, we simplify the system into a piecewise constant (PWC) model. The PWC model has piecewise linear solution and is well suited for theoretical analysis. Basic classification of the synchronous phenomena is given. Using the PWC model, we clarify parameters conditions for existence, stability and super-stability of each phenomenon. The ripple reduction property is also discussed. Using a simple test circuit, typical phenomena are verified in the laboratory.

Our results may be developed into general analysis of bifurcation phenomena of large scale switched dynamical systems; and may give useful information for the design of reliable and efficient power sources. We should note that [7] shows a power distributor with a preliminary WTA-based switching for fault tolerance and [8] gives a PWC model of the buck converter.

2. INTERLEAVED CONVERTERS

Fig. 1 shows the interleaved converters: \( N \) buck converters \( (N \geq 2) \) are interleaved between voltage source \( V_1 \) and a load. The \( j \)-th converter, \( j \in \{1, \cdots, N\} \), includes a current-controlled switch \( S_j \) and an ideal diode \( D_j \). It should be pointed out that, although this paper discusses only the interleaved buck converters, the key idea is applicable also to other types of interleaved buck converters.

The switch \( S_j \) is controlled based on a periodically sampled current \( i_j(nT) \), where \( T \) is a sampling period and \( n \) is a positive integer. In order to define the switching rule, let the \( j \)-th converter be one of the three modes (see Fig.2).

- **Mode 1:** \( S_j=\text{ON}, D_j=\text{OFF} \) and \( 0 < i_j < J_j \)
- **Mode 2:** \( S_j=\text{OFF}, D_j=\text{ON} \) and \( 0 < i_j < J_j \)
- **Mode 3:** \( S_j=\text{OFF}, D_j=\text{OFF} \) and \( i_j = 0 \)
Let the \( j \)-th converter be Mode 1. In this case the current \( i_j \) increases to a threshold \( J_j \). At the moment when \( i_j \) reaches \( J_j \), the converter is changed into Mode 2 and is connected to the load. Let the converter be Mode 2. In this case, \( i_j \) decreases to zero. If \( i_j > 0 \) and \( i_j \) is the minimum at \( t = nT \) among all the currents then the converter is changed into Mode 1 at \( t = nT \) and is connected to the source. If \( i_j \) reaches zero then the converter is changed from Mode 2 to Mode 3. Let the converter be Mode 3. In this case the current \( i_j \) is the minimum and thus the converter is changed into Mode 1 at next sampling time \( t = nT \). The switching rule is summarized as the following:

\[
\begin{align*}
\text{Mode 1} & \rightarrow \text{Mode 2} \quad \text{if} \quad i_j = J_j \\
\text{Mode 1} & \rightarrow \text{Mode 1} \quad \text{if} \quad t = nT \quad \text{and} \quad i_j = \min \\
\text{Mode 2} & \rightarrow \text{Mode 3} \quad \text{if} \quad i_j = 0 \\
\text{Mode 3} & \rightarrow \text{Mode 3} \quad \text{if} \quad t = nT,
\end{align*}
\]

For simplicity, we assume that the time constant \( RC \) is much greater than the sampling period \( T \) and replace the load with a constant voltage source \( V_2 \). The circuit dynamics is described by Equation (2).

\[
L_j \frac{d}{dt} i_j = \begin{cases} 
V_1 - V_2 & \text{for Mode 1} \\
-V_2 & \text{for Mode 2} \\
0 & \text{for Mode 3}
\end{cases}
\]

(Equation 2)

The output current is given by \( I_o = \sum_{j=1}^{N} i_j \). Note that Equation (2) is a PWC model and the solution is piecewise linear: the exact piecewise solution is calculated easily. In Refs. [8, 11], such simplification is used effectively to analyze bifurcation phenomena. We regard the converter with the minimum sampling current as a winner at the sampling moment and refer to this switching rule as to be WTA-based. Note that plural winners can exist for Mode 3: if plural converters are Mode 3 at \( t \in ((n - 1)T, nT] \), then they are winners at \( t = nT \) and are changed into Mode 1. If the system operates to (not to) include Mode 3 then the system is said to operate in a discontinuous conduction mode (DCM) (continuous conduction mode (CCM)).

Using the dimensionless variables and parameters

\[
\tau = \frac{t}{T}, \quad x_j = \frac{i_j}{J_j}, \quad a_j = \frac{T}{L_j J_j} (V_1 - V_2), \quad b_j = \frac{T}{L_j J_j} V_2.
\]

(Equation 3)

Fig. 2. Switching rules

Fig. 3. Typical synchronous phenomena \(((a_j, b_j) = (a, b), j \in \{1, 2, 3\})\). (a) 3-phase synchronization in CCM for \((a, b) = (0.76, 0.38)\). \( R_e = 0 \). (b) 3-phase synchronization in DCM for \((a, b) = (0.69, 0.46)\). \( R_e = 0.30 \). (c) 2-phase synchronization in DCM for \((a, b) = (0.16, 0.10)\). \( R_e = 1.4 \).

Equations (1) and (2) are transformed into

\[
\frac{d}{d\tau} x_j = \begin{cases} 
\frac{a_j}{b_j} & \text{for Mode 1} \\
0 & \text{for Mode 2} \\
0 & \text{for Mode 3}
\end{cases}
\]

(Equation 4)

\[
\begin{align*}
\text{Mode 1} & \rightarrow \text{Mode 2} \quad \text{if} \quad x_j = 1 \\
\text{Mode 2} & \rightarrow \text{Mode 1} \quad \text{if} \quad \tau = n \quad \text{and} \quad x_j = \min \\
\text{Mode 2} & \rightarrow \text{Mode 3} \quad \text{if} \quad x_j = 0 \\
\text{Mode 3} & \rightarrow \text{Mode 1} \quad \text{if} \quad \tau = n
\end{align*}
\]

Note that this dimensionless equation is characterized by \( 2N \) parameters: \((a_1, b_1) \cdots (a_N, b_N)\). The dimensionless output is given by \( X(\tau) = \frac{\sum_{j=1}^{N} J_j x_j(\tau)}{\sum_{j=1}^{N} J_j} \). If \( X \) is periodic with period \( T_p \), \( X(\tau + T_p) = X(\tau) \), we characterize ripple of \( X \) by ripple quantity

\[
R_q = \max_{\tau} X(\tau) - \min_{\tau} X(\tau), \quad 0 \leq \tau < T_p.
\]

(Equation 5)

Fig. 3 shows typical phenomena for \( N = 3 \). In Fig. 3 (a) we can see that the WTA-based switching can distribute phases...
and the system exhibits 3-phase synchronization with ripple reduction. The DCM may be inconvenient for the ripple reduction, however the system can exhibit interesting phenomena, e.g., 3-phase synchronization (Fig.3(b)), 2-phase synchronization having two winners at \( \tau = 2n \) (Fig.3(c)), and chaos (laboratory data in Fig.6. No theory so far).

3. SYNCHRONOUS PHENOMENA

We define synchronous phenomena and their stability.

**Definition 1:** The system is said to have **N-phase synchronous state** (N-SYN) with period N if the following is satisfied in the steady state:

\[
\begin{align*}
x(\tau) &= x(\tau + N), \quad x \equiv (x_1, \cdots, x_N) \\
x_j(\tau) &= x_k(\tau) \quad (k \neq j) \quad \text{at} \quad \tau = p(j),
\end{align*}
\]

where \( p(j) \in \{1, \cdots, N\} \) is a switching instant at which \( x_j \) is the unique winner and is equivalent to an image of a permutation from \( \{1, \cdots, N\} \) onto itself. The \( j \)-th converter is switched from Mode 2 to Mode 1 at \( t = p(j)/T \). In Fig. 3(a) 3-SYN is characterized by \( (p(1), p(2), p(3)) = (2, 3, 1) \).

**Definition 2:** The system is said to have a **M-phase overlapping synchronous state** (M-OSYN) with period M if the following is satisfied in the steady state:

\[
\begin{align*}
x(\tau) &= x(\tau + M), \quad M \in \{1, \cdots, N - 1\} \\
x_j(\tau) &= 0 \quad \text{at} \quad \tau = q(j),
\end{align*}
\]

where \( q(j) \in \{1, \cdots, M\} \) is a switching instant at which \( x_j \) is a winner and is equivalent to an image of a transformation from \( \{1, \cdots, N\} \) onto \( \{1, \cdots, M\} \). The M-OSYN is possible only in the DCM and the \( j \)-th converter is switched from Mode 3 to Mode 1 at \( t = q(j)/T \). If \( q(j) \) has plural preimages then plural winners can exist at \( \tau = q(j) \). In Fig.3(c) 2-OSYN is characterized by \( (q(1), q(2), q(3)) = (1, 2, 2) \).

**Definition 3:** Let \( x_p = (x_{p1}, \cdots, x_{pN}) \) be a solution of Equation (4) for a synchronous state (N-SYN or M-OSYN). The synchronous state is said to be **stable** if

\[
x(\tau) \rightarrow x_p(\tau) \quad \text{for} \quad x(0) = x_p(0) + \epsilon(0),
\]

where \( \epsilon(0) \) is a small initial perturbation. The synchronous state is said to be **super-stable** if

\[
x(\tau) = x_p(\tau) \quad \text{for} \quad x(0) = x_p(0) + \epsilon(0), \quad \text{and} \quad \tau > \tau_f
\]

where \( \tau_f > 0 \) is a finite time.

**Theorem 1:** The system has N-SYN in CCM if

\[
N < a_j^{-1} + b_j^{-1} < \frac{N}{B_{\text{max}}}
\]

where \( B_{\text{max}} = \max_k \left( \frac{N}{a_k^2 - d_k^2} - b_k \right), \quad k \in \{1, \cdots, N\} \).

The N-SYN is stable if \( 0 < b_j < a_j \) and is unstable if \( 0 < a_j < b_j \).

The system has super-stable N-SYN in DCM if

\[
N - 1 < a_j^{-1} + b_j^{-1} < N
\]

The number of the stable (or super-stable) N-SYNs is \( N! \).

**Theorem 2:** The system has super-table M-OSYN if

\[
M - 1 < a_j^{-1} + b_j^{-1} < M, \quad M \in \{1, \cdots, N - 1\}
\]

The number of the stable M-OSYNs is given by

\[
\sum_{j=1}^{K} \frac{N!}{Z_1 Z_2 \cdots Z_{M_j}}
\]

where \( (Z_1, \cdots, Z_{M_j}) \) is an integer solution of Equation (9) and \( K \) is the number of the solutions.

If plural stable (or super-stable) synchronous phenomena exist, the system exhibits one of them depending on the initial state. These theorems can be proven simply using the piecewise linear solution of Equation (4). Fig.4 illustrates Conditions (8) - (10) for \( (a_i, b_i) = (a, b) \) and \( N = 3 \) where Condition (8) is simplified into \( 3 < a_j^{-1} + b_j^{-1} \).

4. EXPERIMENTS

Fig.5 shows an equivalent circuit of the control module that realizes “WTA-based switching” in Fig.1. The IVC transforms each inductor current into a voltage, and the voltage is applied to the WTA and a comparator. The WTA realizes sampling and winner detection: its concrete implementation example can be found in [7]. The outputs of the WTA and the comparators are applied to set and reset terminals of the N flip-flops, respectively. The outputs of the flip-flops control switches \( S_1 \) to \( S_N \) in Fig.1. Using this circuit for \( N = 3 \) we have verified 3-SYN in CCM and 2-OSYN (Fig.6 (a) and (b)). We have also observed chaotic behavior (Fig.6 (c)) of the region "Unstable" in Fig.4. This equivalent circuit is aimed at basic laboratory experiments and the design should be modified for practical applications.
5. CONCLUSION

We have studied a variety of synchronous phenomena from the interleaved buck converters using WTA-based switchings. The number and kinds of the phenomena are clarified and the results are summarized into conditions of dimensionless parameters. Using a simple test circuit, typical phenomena are verified in the laboratory. Future problems include more detailed analysis of bifurcation phenomena, development of efficient control method for practical applications and design of a practical circuit.

6. REFERENCES


